REMARKS

By this amendment, claims 1, 3, and 4 have been amended. Accordingly, claims 1-27, 31-40, 42, and 43 are pending in the present application. The claim amendments are supported by the specification, the accompanying figures, and claims as originally filed, with no new matter being added. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

Due to the lengthy nature of the Office Action, the rejections are grouped and addressed as follows:

1. Examiner's Response to the Applicants Prior Amendments and Arguments

Applicants respectfully thank the Examiner for the provided comments, which allow the Applicant to understand the basis for the rejections and formulate an appropriate response. However, regarding paragraph 16 of this section, "Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection," Applicants respectfully request clarification.

On pages 2-3 of the outstanding Office Action the Examiner incorporates by reference seventeen prior grounds for rejection. Applicants respectfully note that rejections 4-17 do not appear to have been rendered "moot in view of the new ground(s) of rejection" because they are again presented in the outstanding Office Action. Therefore, reconsideration of and an explanation of the Examiner's bases for rejecting the Applicants prior and current arguments regarding these rejections is respectfully requested.

2. Objection Under 37 C.F.R. § 1.75(c)

Claims 2-4 have been objected to under 37 C.F.R. § 1.75(c) for being of improper dependent form for failing to further limit the subject matter of a previous claim. In particular, claim 2 has been objected to for the reason set forth on page 2 of the Office Action dated September 7, 2001, which states: "[T]he rounding the top edge of the trench is an inherent result of forming the liner. Thus, claim 2 do[es] [sic] not appear to further limit[] [sic] claim 1." (Underlining in original).

Although Applicants disagree with the objection, Claims 1, 3, and 4 have been amended and claim 2 has been cancelled to further the prosecution of this case. In particular, claim 1 now recites the limitations of former claim 2 regarding the formation of a liner and claims 3 and 4 now depend from claim 1. Applicants therefore respectfully request the prompt removal of this objection.

3. Rejections Under 35 U.S.C. §§ 112(1) and 132

Claims 1-27, 31-40, 42, and 43 have been rejected under 35 U.S.C. § 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time of the application was filed, had possession of the claimed invention for the reasons stated on page 3 of the Office Action dated September 7, 2001 and pages 4-6 of the Office Action dated May 3, 2002. Applicants respectfully traverse.

Various of the rejected claims have been rejected over some form of the limitation: "wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench." *See e.g.* claim 1. Applicants again cite below, by way of illustration but not as interpretive limitations, instances of support in the Application as filed for these claim recitations.

Operations such as planarizing and selective removing are performed by chemical mechanical planarization or polishing (CMP) in embodiments of this invention that are disclosed in the Application. See, e.g., Application, p. 3, ll. 25-26, p. 6, ll. 1-3, p. 15, l. 4, p. 20, ll. 15-17. The practice of CMP does not rely on masking, but it is known in contrast for its use to achieve an overall planar surface, sometimes referred to as global planarity. A rotating table typically holds the wafer in this CMP process and an appropriate slurry is supplied between the wafer and a polishing pad that is applied to the wafer at a specified pressure. Applicants submit that this knowledge of a person of ordinary skill in the art together with the disclosure in the Application of CMP for selective removing and/or planarizing show possession of the claimed invention.

Independent claims 7 and 42 have been rejected over the limitation: "planarizing with a single etch recipe." Applicants incorporate by reference their prior comments regarding this rejection and in particular emphasize the support found in the term "the single etchback uses **an** etch recipe." Application, p. 17, ll. 9-10 (emphasis added). Applicants submit that this illustrative expression provides support for the use of the terms "single etch recipe" and that it shows possession of the claimed invention to a person of ordinary skill in the art.

The claims have also been rejected for including the recitation, "depositing is carried out to the extent of leaving no gap in each said isolation trench." In response, Applicants note that claim amendments need not necessarily be exact quotations from the specification. Accordingly, Applicants direct the Examiner to page 13, lines 22-24 and page 18, line 25 to page 19, line 1 as well as Figures 6A and 6B of the application as filed. This support clearly indicates to one skilled in the art that the Applicant was in possession of the above claim limitation at the time the application was filed.

Claims 4, 16, and 21 have been rejected for reciting under 35 U.S.C. § 112, first paragraph, "because the specification . . . does not reasonable provide enablement for rounding the top edge of trench by depositing material on the trench surface." Applicants respectfully traverse.

In response, Applicants note that claims 4, 16, and 21 recite the formation of a liner and the step of rounding the top edge of the trench as separate limitations. Further, neither the claims nor the specification require that the step of rounding the top edge of the trench be performed by depositing material. Accordingly, enablement of "rounding the top edge of trench by depositing material on the trench surface" is not necessary and the prompt removal of this rejection is respectfully requested.

Claims 14-17 and 21-23 have been rejected for reciting under 35 U.S.C. § 112, first paragraph, "because the specification . . . does not reasonable provide enablement for depositing CVD, the liner 30 to be confined within each isolation trench." Applicants respectfully traverse.

Initially, Applicants note that claims 14 and 21 recite, "forming a liner" and not "depositing CVD," as suggested by the Office Action. Nevertheless, support for this limitation can be found, *e.g.*, in the application as filed at page 12, line 14-16, which states "CVD of a dielectric material, or a dielectric precursor material that deposits preferentially upon sidewall 50 of isolation trench 32. Thus, at least one exemplary method, the particulars of which are well known in the art is referenced in the specification for forming a liner within a trench. Such a method would be understood as including steps not expressly recited in the specification. Accordingly, the prompt removal of this rejection is respectfully requested.

Applicants therefore respectfully request the prompt withdrawal of the foregoing rejection of the claims under 35 U.S.C. § 112, first paragraph.

4. Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1-26 and 31-40 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner has inquired as to the meaning of, "wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches." Applicants respectfully traverse.

Applicants direct the Examiner to Figure 9 of the application as filed, wherein a plurality of isolation trenches are depicted having continuous material(s) extending into and connecting each isolation trench. As further depicted in Figure 5-8, it can be seen that this continuous material(s) is derived from the electrically insulative materials oxide layer 14, spacer 28, and isolation film 36. Accordingly, the prompt removal of this rejection is respectfully requested.

Claims 21-23 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention and as failing to correspond in scope to what Applicants regard as the invention. In particular, the Examiner states that the phrase "electrically conductive material" lacks antecedent basis. Applicants respectfully traverse.

Claim 21 has been amended to recite: "wherein said conformal third layer is composed of an electrically insulative [conductive] material." Accordingly, the prompt removal of this rejection is respectfully requested.

5. Rejections Based Primarily on U.S. Patent No. 6,184,108

Claims 1-17 and 35-40 have been rejected under either 35 U.S.C. § 102(e) or 35 U.S.C. § 103(a) over U.S. Patent No. 6,184,108 to Omid-Zohoor et al., (hereinafter "the '108 patent") singly or in combination with one or more of U.S. Patent No. 6,097,072 to Omid-Zohoor, et al., (hereinafter "the '072 patent"), U. S. Patent No. 5,387,540 to Poon et al (hereinafter "*Poon*"), and U.S. Patent No. 5,229,316 to Lee et al. (hereinafter "*Lee*") for the reasons stated in the Office Actions dated September 7, 2001 and May 3, 2002. Applicants respectfully traverse.

Regarding the rejections based wholly or in part on the '108 patent, Applicants respectfully request the Examiner to reconsider the Applicants' arguments presented in Amendment and Response "D", incorporated herein by reference, as well as the following.

Independent claims 1 and 7 recite, *inter alia*, "forming a second dielectric layer over said oxide layer and said first dielectric layer " and "wherein each said spacer is situated upon said oxide layer." Claims 1 and 7 also recite "wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas." *See* Figs. 4A-4B and p. 11.

In contrast, the '108 patent discloses an oxide etch to remove the portions of pad oxide layer 42 that are exposed at regions 48, as shown in Fig. 3D therein, and to subsequently deposit spacer oxide layer 50 over the exposed semiconductor substrate 40 at regions 48, as shown in Fig. 3E therein. See also, the '108 patent, col. 4, ll. 3-8. Furthermore, Fig. 3F in the '108 patent shows the formation of sidewall spacers 52 at the sides within exposed regions 48 and at the sides of the terminal portions of pad oxide layer 42 therein. Even if Fig. 3F in the '108 patent did not show the formation of spacers 52 as indicated, such spacers in the '108 patent cannot be situated upon pad

oxide layer 42 because spacers 52 are formed within exposed regions 48 and it is precisely within these regions that pad oxide layer 42 been removed by an oxide etch as indicated above. Therefore, even if, *arguendo*, the layers disclosed in the '108 patent could be analogized with those recited in the rejected claims, the present claims are not anticipated by the '108 patent.

Independent claim 38 recites, *inter alia*, "having a spacer ... upon said oxide layer in contact with said first layer" and "wherein said filling is performed by depositing said second layer and said depositing is carried out to the extent of leaving no gap within each said isolation trench and extending over said spacer and over said first layer." See, e.g., Application, p. 13, ll. 22-24, p. 18, ll. 25-26, p. 19, l. 1. In contrast, the '108 patent discloses a spacer that is not upon any oxide layer, but that it is instead directly on top of semiconductor substrate 40. Furthermore, the '108 patent discloses the formation of a layer within gap 60 that is required not to fill such gap to be able to accommodate a subsequent oxidative process. Therefore, even if, *arguendo*, the layers disclosed in the '108 patent could be analogized with those recited in the rejected claim, the present claim is not anticipated by the '108 patent.

Furthermore, Applicants also reiterate that the '108 patent does not teach or suggest the selectivity rates as recited in claims 9, 10, 12, and 13. The '108 patent discloses the formation of polishing mask 44' and oxide region 66' by polishing oxide region 66 and nitride layer 44, but it is silent as to any selectivity rate, particularly regarding etching the first dielectric layer faster than the conformal layer. See the '108 patent, Fig. 3L, col. 5, ll. 40-46. Hence, the '108 patent does not provide any teaching or suggestion that discloses the selectivity rates that are recited in the pending claims.

Additionally, the Office Action asserts that the '108 patent teaches all the features of claim 14

except for one feature with respect to which *Poon* is cited therein. Applicants respectfully submit that claim 14 is patentable over the '108 patent for at least the reasons presented hereinabove with respect to claim 7 because *Poon* cannot cure the above identified deficiencies of the '108 patent.

Furthermore, *Poon* does not teach or suggest forming a liner upon a sidewall of each said isolation trench, said liner being confined within each said isolation trench and extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate, and consequently *Poon* does not teach or disclose the presently claimed methods with the features recited in claim 14.

Claim 35 recites, *inter alia*, "forming a polysilicon layer upon said oxide layer." The '108 patent has no such teaching or suggestion. Accordingly, the prompt removal of the rejection of claims 35-37 is respectfully requested.

Accordingly, Applicants respectfully request the prompt removal of the foregoing rejections under 35 U.S.C. §§ 102 and 103 based primarily upon the '108 patent.

6. Rejections Based Primarily on U.S. Patent No. 6,097,072

Claims 1-27, 31-38, 42, and 43 have been rejected under one or more of 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a) over the '072 patent singly or in combination with one or more of S. Wolf, *Silicon* Processing, *Poon*, and *Lee* for the reasons stated in the Office Actions dated September 7, 2001 and May 3, 2002. Applicants respectfully traverse.

Present claims 1, 7, 18, 24-26, 31, and 43 recite, *inter alia* and with language variations in each claim, "planarizing the *conformal layer* ... to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (emphasis added).

In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse-resist mask 368 over trench regions 356 (*see* the '72 patent, Fig. 3K, col. 4, *ll.* 51-52) to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a remaining oxide layer 364 with ridges 373 (*see* the '72 patent, Fig. 3L, col. 4, *ll.* 52-54). It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing until silicon nitride layer 344 is exposed (*see* the '72 patent, Fig. 3M, col. 4, *ll.* 54-57, 59-61). Accordingly, the method disclosed in the '072 patent does not *planarize the conformal oxide layer* 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps.

Additionally, present claims 7 and 42 recite the use of a single etch recipe to form a planar upper surface from the conformal layer. In contrast, the method disclosed in the '072 patent, as previously noted, uses a multi-step method with different etch recipes to form a planar upper surface.

Further, claims 1, 7, 14, 18, 24-26, 31, 35, 38, and 42 recite some form of planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, the '072 patent discloses a more complicated method that involves masking of a conformal layer and other steps.

Furthermore, the '072 patent does not teach or suggest forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces. Consequently, the '072 patent does not teach or suggest the presently claimed methods with the features recited in claim 34.

The rejections of the dependent claims that are not specifically addressed herein are rendered

moot by the foregoing traversal of the independent claims.

Accordingly, Applicants therefore respectfully request that the rejection of the claims based primarily on the '072 patent be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 2nd day of January 2002.

Respectfully submitted,

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VERSION WITH MARKINGS SHOWING THE CHANGES MADE

In the claims:

1. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer over [on] and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

forming a liner upon a sidewall of each said isolation trench;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer; and

planarizing the conformal layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

3. (Once Amended) A method according to Claim 1 [2], wherein said a liner is a thermally grown oxide of said semiconductor substrate.

4. (Once Amended) A method according to Claim 1 [2], wherein forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter.